In the Claims

1. - 16. (canceled)

17. (previously presented) A method of fabricating silicon nitride spacers on an integrated circuit device comprising:

providing a semiconductor substrate assembly comprising:

first and second vertically-oriented integrated circuit structures, each having a top and vertical surfaces, wherein said first and second integrated circuit structures are horizontally spaced from each other; and

a horizontal base surface interposed between said first and second integrated circuit structures;

forming a layer of silicon nitride over said top and vertical surfaces of each of said first and second integrated circuit structures such that said top and vertical surfaces of first and second integrated circuit structures and said horizontal base surface between said integrated circuit structures are covered with said layer of silicon nitride; and

anisotropically etching said layer of silicon nitride over said top surfaces of said first and second integrated circuit structures and over said horizontal base surface with an etchant consisting essentially of oxygen at a flow rate of between about 20 sccm to about 80 sccm and CHF_3 at a flow rate of between about 5 sccm to about 25 sccm, such that said flow rates of oxygen and CHF_3 have a ratio of about three to one (3:1) and provide a vertical to horizontal etch rate of about four to one (4:1) to result in silicon nitride spacers on said vertical integrated circuit structure.

18. (previously presented) A method of fabricating silicon nitride spacers on an integrated circuit device comprising:

providing a semiconductor substrate assembly comprising:

first and second vertically-oriented integrated circuit structures, each having a top and vertical surfaces, wherein said first and second integrated circuit structures are horizontally spaced from each other; and

a horizontal base surface interposed between said first and second integrated circuit structures;

forming a layer of silicon nitride over said top and vertical surfaces of each of said first and second integrated circuit structures such that said top and vertical surfaces of first and second integrated circuit structures and said horizontal base surface between said integrated circuit structures are covered with said layer of silicon nitride; and

anisotropically etching said layer of silicon nitride over said top surfaces of said first and second integrated circuit structures and over said horizontal base surface with an etchant consisting essentially of oxygen at a flow rate of between about 20 sccm to about 80 sccm and CH_2F_2 at a flow rate of between about 5 sccm to about 25 sccm, such that said flow rates of oxygen to CH_2F_2 have a ratio of about three to one (3:1) and provide a vertical to horizontal etch rate of about four to one (4:1) to result in silicon nitride spacers on said vertical integrated circuit structure.